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L34	L30 and l10	28	L34
L33	L30 and l8	310	L33
L32	L30 and l7	310	L32
L31	L30 and l9	79	L31
L30	l20 and modulo	310	L30
L29	l20 and strid\$3	32	L29
L28	L20 and l13	7	L28
L27	L20 and l12	29	L27
L26	L20 and l11	12	L26
L25	L20 and l10	45	L25

<u>L24</u>	L20 and 19	141	<u>L24</u>
<u>L23</u>	L20 and 18	521	<u>L23</u>
<u>L22</u>	L20 and 17	521	<u>L22</u>
<u>L21</u>	L20 and 19	141	<u>L21</u>
<u>L20</u>	17 and 18	521	<u>L20</u>
<u>L19</u>	17 and 113	14	<u>L19</u>
<u>L18</u>	17 and 112	57	<u>L18</u>
<u>L17</u>	17 and 111	24	<u>L17</u>
<u>L16</u>	17 and 110	100	<u>L16</u>
<u>L15</u>	17 and 19	344	<u>L15</u>
<u>L14</u>	16 and 17	1433	<u>L14</u>

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<u>L13</u>	(711/216-221)[CCLS]	2061	<u>L13</u>
<u>L12</u>	(711/201-221)[CCLS]	7062	<u>L12</u>
<u>L11</u>	(712/2-8)[CCLS]	469	<u>L11</u>
<u>L10</u>	(712/2-24)[CCLS]	2960	<u>L10</u>
<u>L9</u>	(712/2-300)[CCLS]	13995	<u>L9</u>

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<u>L8</u>	(arbitr\$6 or random\$4) near12 (address\$6)	44530	<u>L8</u>
<u>L7</u>	L6 and (increment\$3 or decrement\$3 or trid\$3 or modulo)	1433	<u>L7</u>
<u>L6</u>	L5 and (updat\$5 or modif\$7)	1994	<u>L6</u>
<u>L5</u>	L4 and (valid\$1 or invalid\$7) near12 (entr\$4 or column\$1 or row\$1)	2124	<u>L5</u>
<u>L4</u>	L1 11 near50 (column\$1 or row\$1 or array or matrix or mtrices)	74576	<u>L4</u>
<u>L3</u>	r mtricesL2	8308712	<u>L3</u>
<u>L2</u>	L1 11 near50 (column\$1 or row\$1 or array)	74576	<u>L2</u>
<u>L1</u>	vector\$1 near15 (point\$4 or address\$6 or index\$3 or indices)	74576	<u>L1</u>

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